Fig. 9 illustrates metal lines formed along with the contacts shown in Fig. 8.

Fig. 10 illustrates metals for applying power voltage and grounding voltage to the metal lines.

Replace the paragraph beginning at page 5, line 3 and ending at page 5, line 4 with the following paragraphs:

Fig. 12 illustrates a layout method of the sense amplifier as shown in Fig. 4 in accordance with an embodiment of the present invention.

Fig. 13 illustrates contacts formed in the layout shown in Fig. 12.

Fig. 14 illustrates metals formed at the contacts shown in Fig. 13.

Fig. 15 illustrates contacts formed at the metals shown in Fig. 14.

Fig. 16 illustrates metal lines formed along with the contacts shown in Fig. 15.

Replace the paragraph beginning at page 5, line 18 and ending at page 5, line 22 with the following paragraph:

However, there is a problem in the conventional layout method of neighboring circuits of the semiconductor device in that the transistor gates of the neighboring circuits have been arranged at an irregular gap in the conventional layout method of the semiconductor device, thereby increasing variances in process deviations at the transistor gates in the course of the photo and etching processes.

IN THE ABSTRACT

Please amend the Abstract as follows:

A semiconductor device layout involving the following: arranging active regions of a plurality of transistors having at least more than one first and second electrodes disposed on a substrate; arranging a plurality of gates of transistors between more than one first and second electrodes of those active regions respectively by positioning at least more than one gates having predetermined width and length at a constant gap on the substrate; and arranging a plurality of dummy gates having predetermined width and length between a plurality of transistors (or between and outside transistors) at the same gap as that of the gates of transistors on the substrate, so that all the gates of transistors are arranged at a constant gap to minimize the variance of process deviations and accordingly reduce the difference of threshold voltage of transistors, thereby increasing reliability of the semiconductor device.